

## **REMARKS**

In the 12 July 2006 *Office Action*, the Examiner rejects all pending claims, Claims 1-20. In response, Applicant clarifies certain of Applicant's claims by the above-presented amendments.

Applicant thanks the Examiner with appreciation for the careful consideration and examination given to the Application. The undersigned respectfully requests a telephonic conference with the Examiner regarding the above-presented amendments, following remarks, and the cited references.

After entry of this Response, Claims 1-20 are pending in the Application. Applicant respectfully asserts that Claims 1-20 are in condition for allowance and respectfully request reconsideration of the claims in light of the following remarks.

### **I. Pending Claims & Present Rejections**

As the Examiner will recall, embodiments of Applicant's invention can provide an apparatus that reads a memory location more than once in response to receiving invalid data from the memory location. Also, advantageously, the memory location can be read again (e.g., at least a second time) before a subsequent transaction (such as a write transaction) occurs at the memory location initially providing invalid data. (*Specification*, Paragraphs 6-10). In addition, Applicant's claimed invention enables a memory system to flag a memory location as providing invalid data so that future write operations to a erroneous memory location is disabled until valid data is read from the erroneous memory location. (*Specification*, Paragraphs 39-40).

As discussed in detail below, Applicant respectfully submits that the references of record do not render Applicant's claims unpatentable. That is, Applicant respectfully asserts that the cited references do not teach to read a memory location again after an initial read resulted in invalid data coming from the memory location (see claims for exact language). Applicant also respectfully asserts that the cited references do not disclose an apparatus adapted to: dispatch a pending transaction to a device, dispatch a device read transaction resulting in an invalid data signal and, subsequently, to that sending to a desired destination a data available signal for data resulting from a device read transaction which was dispatched again, and dispatch a pending transaction to the device. For at least these reasons and the below-discussed reasons, Applicant respectfully asserts that Claims 1-20 are patentable over the cited references.

## **II. 35 U.S.C. § 102 Rejection**

The Examiner rejects Claims 1-14, 16-18 and 20 under 35 U.S.C. § 102(b) as allegedly being anticipated by *Hagerston* (USPN 5,829,033). The Examiner asserts that *Hagerston* discloses the subject matter contained in Claims 1-14, 16-18 and 20. Applicant respectfully traverses the § 102 rejection especially in light of the above-presented amendments because *Hagerston* does not disclose each and every claimed element and limitation as required by § 102(b), and thus does not support a prima facie case of anticipation required by MPEP 2131..

*Hagerston* discloses a system for optimizing responses in a coherent distributed electronic system including a computer system. A main objective of *Hagerston's* system is to provide a system for updating cache memory systems to include the same data so that multiple caches are coherent. (Column 3, Lines 1-45). *Hagerston's* system provides a ReadToShareFork (“RTSF”) transaction that simultaneously causes a write-type operation that updates invalid data from a requested memory address, and provides the updated data to the requesting device. (Column 5, Lines 34-45).

The Examiner asserts that this RTSF transaction teaches certain elements of Applicant's claimed invention, and Applicant respectfully disagrees with this assertion in light of the clarifying amendments presented above. More specifically, *Hagerston* states that the valid data is returned to the requestor whose data request is still outstanding. In other words, the RTSF function provides data to a requesting device after an initial read but the actual read operation to the memory location that provided invalid data does not occur again such that the memory location is read multiple times as claimed by Applicant. In short, the RTSF function does not access or read a memory device or data location again to obtain valid data; rather the RTSF function “provides the updated data to the requesting device.” Accordingly, since *Hagerston* does not teach or disclose this claimed feature of Applicant's claimed invention, Applicant respectfully asserts that Applicant's claimed invention is patentable over *Hagerston*.

Applicant also respectfully asserts that Claims 13 and 17 are allowable for additional reasons. Both Claims 13 and 17 recite “inhibiting write operations to the device.” The Examiner asserts that Column 24, Lines 65-67 teach such claimed feature. This disclosure, however, does not disclose inhibition of write operations; rather it discloses a coding scheme permitting devices to distinguish between error types. (Column 25, Lines 1-2).

Applicant also respectfully asserts that certain dependent claims are allowable. For example, Claims 6 and 16 are not anticipated by *Hagerston*. The Examiner asserts that a portion of *Hagerston* that reads: “The Mapped signal preferably allows sufficiently lengthy timeouts to be treated as fatal hardware errors rather than as nonfatal errors” anticipates Claims 6 and 16. Such is not the case. Claims 6 and 16 recite that the invalid data has an uncorrectable error. This portion of *Hagerston* fails to even mention data, much less data having an uncorrectable error. Accordingly Claims 6 and 16 are patentable over *Hagerston*.

For at least these reasons, Applicant respectfully asserts that Claims 1-20 are allowable over *Hagerston*. Therefore, withdrawal of the § 102(b) rejections are respectfully requested.

### **III. 35 U.S.C. § 103 Rejection**

The Examiner asserts that Claims 15 and 19 are unpatentable under 35 U.S.C. § 103. Specifically, the Examiner asserts that a combination of *Hagerston* and *Brzezinski* (USPN 5,570,297) renders Claims 15 and 19 unpatentable.

Applicant respectfully traverses the § 103 rejections in light of the above-presented remarks regarding *Hagerston*. Because *Hagerston* fails to teach each and every claimed limitation of the independent claims and *Brzezinski* does not overcome the deficiencies of *Hagerston*, the asserted § 103 rejection also fails to teach the subject matter as a whole as claimed in dependent Claims 15 and 19. Accordingly, Applicant respectfully asserts that Claims 15 and 19 are allowable over the cited combination for at least this reason.

Applicant also respectfully asserts that Claim 15 and 19 are allowable for additional reasons. Applicant respectfully submits that the Examiner has not set forth a *prima facie* case of obviousness. As MPEP § 2143 provides, a *prima facie* of obviousness requires three findings. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art must teach or suggest all the claim limitations.

Here, the cited combination fails to teach each and every limitation and feature as Applicant claims in Claims 1-20. Accordingly, the Examiner has not set forth a *prima facie* case of obviousness. Applicant, therefore, respectfully submits that Claims 15 and 19 are allowable over the cited combination. Withdrawal of the § 103 rejection is respectfully requested.

**IV. Fees & Express Request for Continued Examination Under 37 CFR § 1.114**

Applicant files this Response within three months of the 12 July 2006 *Final Office Action* and with no additional claims. Thus, Applicant believes that no extension or claims fees are due.

Applicant hereby expressly requests continued examination pursuant to 37 C.F.R. § 1.114. Applicant submits this submission as the required RCE submission and also pays the appropriate RCE fee via EFS-Web.

No additional fees are believed due. The Commissioner is authorized, however, to charge any fees that may be required, or credit any overpayment, to Deposit Account No. 20-1507 for full acceptance of this submission.

**V. Conclusion**

The foregoing is believed to be a complete response to the *Final Office Action* mailed 12 July 2006. Applicant respectfully asserts that Claims 1-20 are in condition for allowance and respectfully requests passing of this case in due course of patent office business. If the Examiner believes there are other issues that can be resolved by a telephone interview, or there are any informalities remaining in the application which may be corrected by an Examiner's amendment, a telephone call to Hunter Yancey at (404) 885-3696 is respectfully requested.

Respectfully submitted,

TROUTMAN SANDERS LLP

/jameshuntyanceyjr53809/  
James Hunt "Hunter" Yancey, Jr.  
USPTO Registration No. 53,809  
Attorney for INTEL CORPORATION

TROUTMAN SANDERS LLP  
Bank of America Plaza  
600 Peachtree Street, NE  
Suite 5200  
Atlanta, Georgia 30308-2216  
United States of America  
P: (404) 885-3696  
F: (404) 962-6828  
E: hunter.yancey@troutmansanders.com  
**DATE: 12 OCTOBER 2006**